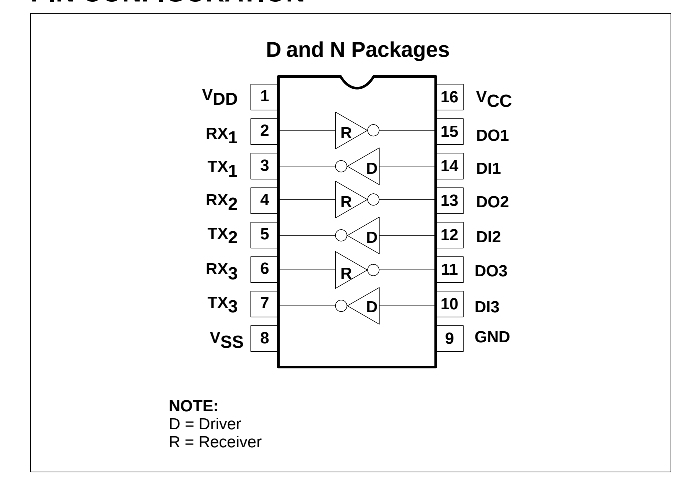
EIA-232-D/V.28 driver/receiver — MC145406

DESCRIPTION

The MC145406 is a silicon-gate CMOS IC that combines 3 drivers and 3 receivers to fulfill the electrical specifications of standards EIA-232-D and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate limited output, 300Ω power-off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ±25V while presenting 3 to 7kΩ impedance. Hysteresis in the receiver aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low-power solutions for EIA-232-D and V.28 applications.

PIN CONFIGURATION



APPLICATIONS

- Modem interface
- Voice/data telephone interface
- Lap-top computers
- UART interface

FEATURES

- **Drivers**
- ±5 to ±12V supply range
- 300Ω power-off source impedance
- Output current limiting
- TTL compatible
- Maximum slew rate = 30V/µs
- **Receivers**
- ±25V input voltage range over the full supply range
- 3 to 7kΩ input impedance
- Hysteresis on input switchpoint
- **General**
- Very low supply currents for long battery life
- Operation is independent of power supply sequencing

ORDERING INFORMATION

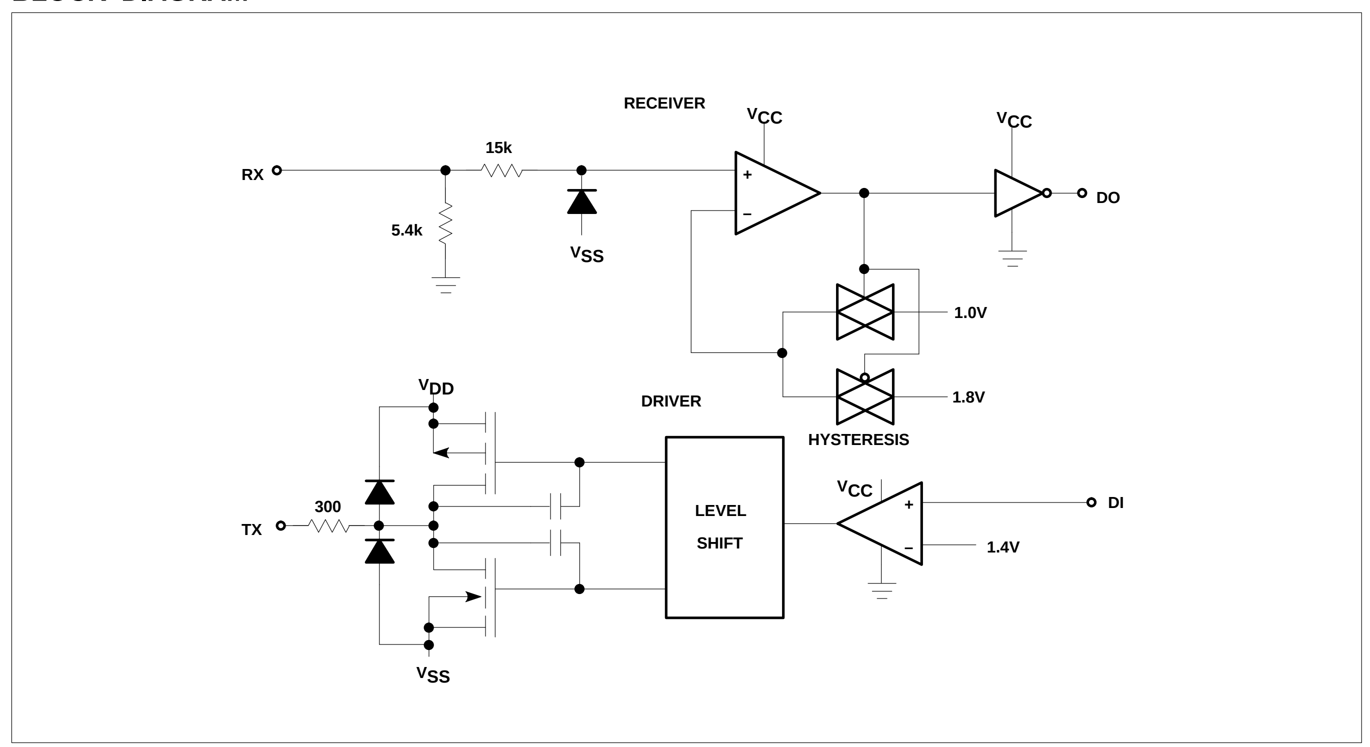
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	MC145406N	0406C
16-Pin Small Outline Large (SOL) Package	0 to +70°C	MC145406D	0171B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +6.0	V
V_{DD}	Supply voltage	-0.5 to +13.5	V
V_{SS}	Supply voltage	+0.5 to -13.5	V
V_{IR}	Input voltage range RX_{1-3} inputs DI_{1-3} inputs	 (V_{SS} - 15) to (V_{DD} + 15) -0.5 to (V_{CC} + 0.5)	V
	DC current per pin	±100	mA
P_D	Power dissipation (package)	1.0	W
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
θ_{JA}	Thermal impedance N package D package	80 105	°C/W

NOTE: This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{DD} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the RX pin should be constrained to ±25V, and TX should be constrained to V_{SS} ≤ V_{TX1-3} ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for RX).

BLOCK DIAGRAM



PIN #	SYMBOL	PIN DESCRIPTION
1	V_{DD}	**Positive power supply**. The most positive power supply pin, which is typically 5 to 12 volts.
8	V_{SS}	**Negative power supply.** The most negative power supply pin, which is typically -5 to -12 volts.
16	V_{CC}	**Digital power supply**. The digital supply pin, which is connected to the logic power supply (maximum +5.5V).
9	GND	**Ground.** Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (Pin 7) as well as to the logic power supply ground.
2, 4, 6	RX_1, RX_2, RX_3	**Receive Data Input.** These are the EIA-232-D receive signal inputs whose voltages can range from +25 to -25V. A voltage between +3 and +25 is decoded as a space and causes the corresponding DO pin to swing to ground (0V); a voltage between -3 and -25V is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8V above ground, and includes 800mV of hysteresis for noise rejection. The nominal input impedance is 5kΩ. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.
11, 13, 15	DO1, DO2, DO3	**Data Output.** These are the receiver digital output pins, which swing from V_{CC} to GND. A space on the RX pin causes DO to produce a logic zero; a mark produces a logic one. Each output pin is capable of driving one LSTTL input load.
10, 12, 14	DI1, DI2, DI3	**Data Input.** These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4V above ground. However, 5V CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and GND.
3, 5, 7	TX1, TX2, TX3	**Transmit Data Output.** These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corresponding TX output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30V/µs. When the MC145406 is off (V_{DD} = V_{SS} = V_{CC} = GND), the minimum output impedance is 300Ω.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +6.0	V
V_{DD}	Supply voltage	-0.5 to +13.5	V
V_{SS}	Supply voltage	+0.5 to -13.5	V
V_{IR}	Input voltage range RX_{1-3} inputs DI_{1-3} inputs	 $(V_{SS}$ - 15) to $(V_{DD}$ + 15) -0.5 to $(V_{CC}$ + 0.5)	V
	DC current per pin	±100	mA
P_D	Power dissipation (package)	1.0	W
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
θ_{JA}	Thermal impedance N package D package	80 105	°C/W

NOTE: This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range GND $\leq V_{DI} \leq V_{DD}$ and GND $\leq V_{DO} \leq V_{CC}$. Also, the voltage at the RX pin should be constrained to ±25V, and TX should be constrained to $V_{SS} \leq V_{TX1-3} \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for RX).

DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DC supply voltage						
V_{DD}			4.5	5 to 12	13.2	V
V_{SS}			-4.5	-5 to -12	-13.2	V
V_{CC}			4.5	5.0	5.5	V
Quiescent supply current (outputs unloaded, inputs low)						
I_{DD}		V_{DD} = +12V		20	400	μA
I_{SS}		V_{SS} = -12V		280	600	μA
I_{CC}		V_{CC} = +5V		260	450	μA

RECEIVER ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V; V_{DD} = +5 to +12V; V_{SS} = -5 to -12V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{ON}	Input turn-on threshold RX_{1-3}	$V_{DO1-3} = V_{OL}$, V_{CC} = 5.0V ±5%	1.35	1.80	2.35	V
V_{OFF}	Input turn-off threshold RX_{1-3}	$V_{DO1-3} = V_{OH}$, V_{CC} = 5.0V ±5%	0.75	1.00	1.25	V
V_{ON}-V_{OFF}	Input threshold hysteresis RX_{1-3}	V_{CC} = 5.0V ±5%	0.6	0.8		V
R_{IN}	Input resistance RX_{1-3}	$(V_{SS}-15V) \leq V_{RX1-3} \leq (V_{DD}+15V)$	3.0	5.0	7.0	kΩ
V_{OH}	High level output voltage DO_{1-3} V_{RX1-3} = -3V to $(V_{SS}$-15V)[1]	I_{OH} = -20μA, V_{CC} = +5.0V	4.9	5.0		V
		I_{OH} = -1mA, V_{CC} = +5.0V	3.8	4.4		
V_{OL}	Low level output voltage DO_{1-3} V_{RX1-3} = +3V to $(V_{DD}$+15V)[1]	I_{OL} = +20μA, V_{CC} = +5.0V		0.005	0.1	V
		I_{OL} = +2mA, V_{CC} = +5.0V		0.15	0.5	
		I_{OL} = +4mA, V_{CC} = +5.0V		0.3	0.7	

NOTE:
1. This is the range of input voltages as specified by EIA-232-D to cause a receiver to be in the high or low logic state.

DRIVER ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
V_{IL}	Digital input voltage	DI_{1-3}	Logic 0			0.8	V
V_{IH}	Digital input voltage	DI_{1-3}	Logic 1	2.0			V
I_{IN}	Input current	DI_{1-3}	$V_{DI1-3} = V_{CC}$			±1.0	μA
V_{OH}	Output high voltage V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = -5.0V	3.5	4.1		V
			V_{DD} = +6.0V, V_{SS} = -6.0V	4.3	5.0		
			V_{DD} = +12.0V, V_{SS} = -12.0V	9.2	10.4		
V_{OL}	Output low voltage[1] V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = -5.0V	-4.0	-4.3		V
			V_{DD} = +6.0V, V_{SS} = -6.0V	-4.5	-5.2		
			V_{DD} = +12.0V, V_{SS} = -12.0V	-10.0	-10.3		
	Off source resistance Figure 1	TX_{1-3}	$V_{DD}=V_{SS}$=GND=0V, V_{TX1-3} = ±2.0V	300			Ω
I_{SC}	Output short-circuit current	TX_{1-3}	TX_{1-3} shorted to GND[2]		±22	±60	mA
	V_{DD} = +12.0V, V_{SS} = -12.0V		TX_{1-3} shorted to ±15.0V[3]		±60	±100	mA

NOTE:
1. The voltage specifications are in terms of absolute values.
2. Specification is for one TX output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.
3. This condition could exceed package limitations.

SWITCHING CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; V_{CC} = +5V ±5%, unless otherwise specified. (See Figures 2 and 3)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
Drivers							
t_{PLH}	Propagation delay time	TX_{1-3}	Low-to-High R_L = 3kΩ, C_L = 50pF		300	500	ns
t_{PHL}	Propagation delay time	TX_{1-3}	High-to-Low R_L = 3kΩ, C_L = 50pF		300	500	ns
SR	Output slew rate (minimum load)	TX_{1-3}	R_L = 7kΩ, C_L = 0pF, V_{DD} = 6 to 12.0V, V_{SS} = -6 to -12V		±6	±30	V/μs
	Output slew rate (maximum load)	TX_{1-3}	R_L = 3kΩ, C_L = 2500pF, V_{DD} = 12V, V_{SS} = -12V		±3.0		
Receivers (C_L = 50pF)							
t_{PLH}	Propagation delay time	DO_{1-3}	Low-to-High		150	425	ns
t_{PHL}	Propagation delay time	DO_{1-3}	High-to-Low		150	425	ns
t_R	Output rise time	DO_{1-3}			120	400	ns
t_F	Output fall time	DO_{1-3}			40	100	ns

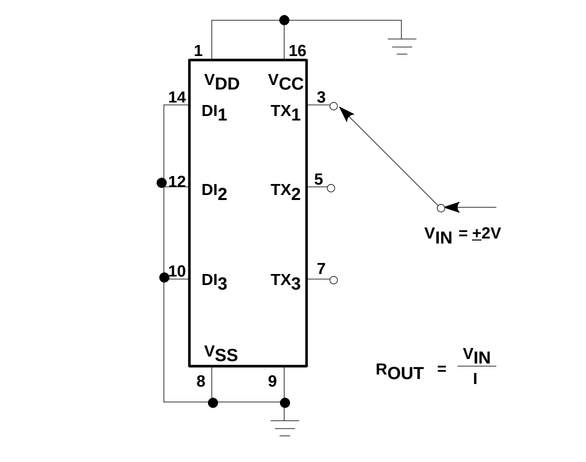


Figure 1. Power-Off Source Resistance (Drivers)

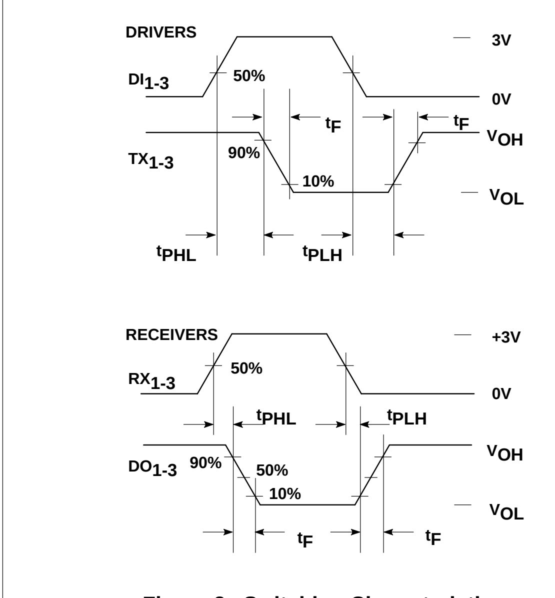


Figure 2. Switching Characteristics

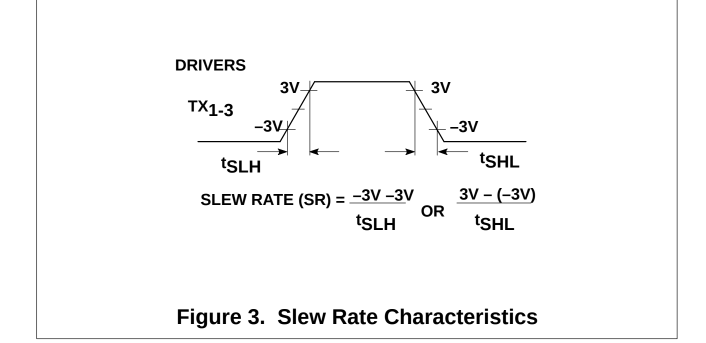


Figure 3. Slew Rate Characteristics

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA-232-D/CCITT V.28 and as such, defines the electrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads, which allow the transfer of timing, data, control, and test signals. The MC145406 provides the necessary level shifting between the TTL/CMOS logic levels and the high voltage levels of EIA-232-D (ranging from ±3 to ±25V).

DRIVERS

As defined by the specification, an EIA-232-D driver presents a voltage of between ±5 to ±15V into a load of between 3 to 7kΩ. A logic one at the driver input results in a voltage of between -5 to -15V. A logic zero results in a voltage between ±5 to ±15V. When operating at ±7 to ±12V, the MC145406 meets this requirement. When operating at ±5V, the MC145406 drivers produce less than ±5V at the output (when terminated), which does not meet the EIA-232-D specification. However, the output voltages when using a ±5V power supply are high enough (around ±4V) to permit proper reception by an EIA-232-D receiver, and can be used in applications where strict compliance to EIA-232-D is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA-232-D cable. The worst-case condition that is permitted by EIA-232-D is a ±15V source that is current limited to 500mA. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300Ω output impedance needed to satisfy the EIA-232-D driver requirements. This will reduce the short circuit current to under 40mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally-limited output slew rate that does not exceed 30V/μs.

RECEIVERS

The job of an EIA-232-D receiver is to level-shift voltages in the range of -25 to +25V down to TTL/CMOS logic levels (0 to +5V). A voltage of between -3 and -25V on RX_1 is defined as a mark and produces a logic one at DO_1. A voltage between +3 and +25V is a space and produces a logic zero. While receiving these signals, the RX inputs must present a resistance between 3 and 7kΩ. Nominally, the input resistance of the RX_{1-3} inputs is 5.0kΩ.

The input threshold of the RX_{1-3} inputs is typically biased at 1.8V above ground (GND) with typically 800mV of hysteresis included to improve noise immunity. The 1.8V bias forces the appropriate DO pin to a logic one when its RX input is open or grounded as called for in EIA-232-D specification. Notice that TTL logic levels can be applied to the RX inputs in lieu of normal EIA-232-D signal levels. This might be helpful in situations where access to the modem or computer through the EIA-232-D connector is necessary with TTL devices. However, it is important not to connect the EIA-232-D outputs (TX_1) to TTL inputs since TTL operates off +5V only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from the digital power supply. The TX and RX sections are independently powered by V_{DD} and V_{SS} so that one may run logic at +5V and the EIA-232-D signals at ±12V.